IN THE CLAIMS

Claims 4, 12, 14, and 15 were objected for informalities. Applicant believes that the proposed amendments to the claims 4, 12, 14, and 15 overcome the Examiner's objection. In addition, the Applicant has carefully reviewed all of the pending claims and has made several proposed amendments to correct for grammatical and/or antecedent basis problems.

The specific amendments to individual claims are detailed in the following marked-up set of claims.

1. (Currently Amended) A charge pump, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators [,] and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

2. (Currently Amended) A charge pump, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; [and]

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second

pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively,

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, [and] wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively, and wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

3. (Currently Amended) A charge pump, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors , wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively[; and], wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during [the] first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level moves [is moved] to a third predetermined level in response to the plurality of phase generators during the first and second phases,

respectively, [and] wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively, and wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

4. (Currently Amended) The charge pump of claim 3, wherein the plurality of phase generators comprises:

a primary phase generator; and

a secondary phase generator coupled to the primary phase generator [;], wherein the first and second preboot capacitors are coupled to the primary phase generator, [;] and the first and second main pump capacitors are coupled to the secondary phase generator [,] and the first and second preboot capacitors, respectively.

5. (Currently Amended) A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

a primary phase generator coupled to the oscillator;

a secondary phase generator coupled to the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the secondary phase generator, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, [; and]

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during [the] first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the primary phase generator during the first and second phases, respectively, wherein the second

predetermined level moves [is moved] to a third predetermined level in response to the secondary phase generator during the first and second phases, respectively, [and] wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively, and wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

6. (Previously Amended) The charge pump of claim 5, further including a power source, wherein the power source includes an output voltage approximately in the range of about 1 to 2.5 volts.

7. (Previously Amended) The charge pump of claim 5, wherein the primary phase generator comprises:

an inverter, coupled to the oscillator to receive an input signal from the oscillator based on the phase cycle and providing output signals which are 180 degrees out of phase; and

cross coupled gates coupled to the inverter to receive the output signals from the inverter and outputting signals that are non-overlapping and crossing around high points of their signals during the first and second phases, respectively, and further outputting signals that are non-overlapping and crossing around low points of their signals during the first and second phases, respectively.

8. (Previously Amended) The charge pump of claim 5, wherein the secondary phase generator comprises a delay circuit coupled to the primary phase generator, including an input receiving signals that are non-overlapping and crossing around high points of their signals from the primary phase generator, and providing an output signal having a predetermined delay from the input signal.

9. (Previously Amended) The charge pump of claim 8, wherein the predetermined delay is approximately in the range of about 10 to 30 nanoseconds.

10. (Currently Amended) The charge pump of claim 8, wherein the first and second preboot capacitors are coupled to the primary phase generator to receive input signals that are non-overlapping and crossing around high points and low points of their signals, and provide an output signal to preboot the first and second main capacitors to the [a] first predetermined level during the first and second phases, respectively.

11. (Previously Amended) The charge pump of claim 10, wherein the first predetermined level is approximately in the range of about 1 to 5 volts.

12. (Currently Amended) The charge pump of claim 10, further comprising first and second precharge capacitors coupled to the primary phase generator and the first and second main pump capacitors, respectively, including an input receiving the signals that are non-overlapping and crossing around high points of their signals and providing an output signal to precharge the first and second main capacitors to the [a] second predetermined level during the first and second phases, respectively.

13. (Previously Amended) The charge pump of claim 12, wherein the second predetermined level is approximately in the range of about 1 to 5 volts.

14. (Currently Amended) The charge pump of claim 12, wherein the first and second precharge capacitors further comprise sharing [comprising] transistors to precharge the first and second precharge capacitors.

15. (Currently Amended) The charge pump of claim 14, wherein the first and second main pump capacitors coupled to the secondary phase generator, and the first and second precharge capacitors, respectively, including an input receiving the delayed signal from the secondary phase generator to move the second predetermined level to the [a] third predetermined level, and dumping an output during the first and second phases, respectively.

16. (Previously Amended) The charge pump of claim 15, wherein the third predetermined level is approximately in the range of about 1 to 5 volts.

17. (Currently Amended) The charge pump of claim 15, wherein the first and second gating devices coupled to the first and second main pump capacitors include [, including] an input to receive [receiving] the dumped signal from the first and second main pump capacitors and an output to receive [outputting] a charge to an external load.

18. (Currently Amended) The charge pump of claim 15, wherein the outputted [outputting] charge is approximately in range of about 1.5 to 5 volts.

19. (Currently Amended) A charge pump, comprising:

an oscillator to generate [a] first and [a] second phases [phase] during a phase cycle;

a primary phase generator coupled to the oscillator;

a secondary phase generator coupled to the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the secondary phase generator, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, [; and] wherein the first and second main pump capacitors are prebooted to a first predetermined level of approximately in the range of about 1 to 5 volts by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level of approximately in the range of about 1 to 5 volts in response to the primary phase generator during the first and second phases, respectively, wherein the second predetermined level is moved to a third predetermined level of approximately in the range of about 1 to 1.5 volts in response to the secondary phase generator during the first and second phases, respectively, [and] wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively,

and wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

20. (Currently Amended) A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

a primary phase generator coupled to the oscillator further includes;

an inverter, coupled to the oscillator to receive an input signal from the oscillator based on the phase cycle and providing output signals which are 180 degrees out of phase; and

cross coupled gates coupled to the inverter to receive the output signals from the inverter and to output [outputting] signals that are non-overlapping and crossing around high points of their signals during the first and second phases, respectively, and further to output [outputting] signals that are non-overlapping and crossing around low points of their signals during the first and second phases, respectively;

a secondary phase generator coupled to the primary phase generator receives the signals that are non-overlapping and crossing around high points of their signals from the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator receives the signals that non-overlapping and crossing around high points and low points of their signals from the primary phase generator, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the secondary phase generator, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, [; and] wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the primary phase generator during the first and second phases, respectively, wherein

the second predetermined level is moved to a third predetermined level in response to the secondary phase generator during the first and second phases, respectively, [and] wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively, and wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

21. (Currently Amended) A charge pump, comprising:

an oscillator to generate a first phase and a second phase during a phase cycle;

first and second primary phase generators coupled to the oscillator;

first and second secondary phase generators coupled to the first and second primary phase generators, respectively;

first and second preboot capacitors coupled to the first and second primary phase generators, respectively, wherein each of the first and second preboot capacitors has an output;

a first main pump capacitor coupled to the first secondary phase generator [,] and the first preboot capacitor;

a second main pump capacitor coupled to the second secondary phase generator [,] and the second preboot capacitor;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

[a] first and second p-channel gates coupled to the first and second main pump capacitors, respectively, [;]

wherein the first main pump capacitor is prebooted to a first pre-determined level by the first preboot capacitor during the first phase, wherein the first pre-determined level moves to a second pre-determined level during the second phase in response to the first primary phase generator, wherein the second predetermined level moves to a third predetermined level in response to the first secondary phase generator, and wherein the third predetermined level dumped to a first p-channel gate during the first phase, [;] and

wherein the second main pump capacitor is prebooted to a first pre-determined level by the second preboot capacitor during the second phase, wherein the first predetermined level

moves to a second pre-determined level during the first phase in response to the second primary phase generator, wherein the second predetermined level moves to a third predetermined level in response to the second secondary phase generator, and wherein the third predetermined level dumped to a second p-channel gate during the second phase, and wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second p-channel gates.

22. (Currently Amended) A charge pump circuit, comprising:

a phase generator to generate [a] first and [a] second phases [phase] during a phase cycle;

a primary phase generator, coupled to the phase generator, wherein the primary phase generator includes [a] first and [a] second phase generators [generator] to generate [a] first and [a] second phase signals [signal] that are non-overlapping and crossing each other substantially around their high points during the phase cycle, wherein the primary phase generator further generates [a] third and [a] fourth phase signals [signal] that are non-overlapping and crossing around their low points during the phase cycle, and wherein the primary phase generator further generates [a] seventh and [a] eighth phase signals [signal];

a secondary phase generator, coupled to the primary phase generator, wherein the secondary phase generator includes [a] first and [a] second secondary phase generators [generator] to generate [a] fifth and sixth phase signals [signal] similar to the first and second phase signals [signal], and including a predetermined delay from the first and second phase signals [signal];

[a] first and [a] second main energy storing devices [device];

[a] first and [a] second pre-boosting stages [stage], coupled to the first and second primary phase generators, respectively, wherein each of the first and second pre-boosting stages has an output, wherein the first and second pre-boosting stages boost [boosts] the first and second main energy storing devices to a first predetermined boost level during the first and second phases respectively; [and]

[a] first and [a] second pre-charging stages [stage], coupled to the first and second main energy storing devices, wherein each of the first and second pre-charging stages has an output, and wherein the output of each of the first and second pre-charging stages is coupled to the output of the first and second pre-boosting stages, respectively; and

first and second gating devices coupled to the first and second main energy storing devices, respectively, wherein the first and second pre-charging stages further boost the first and second main energy storing devices to a second predetermined boost level during the first and second phases, respectively, wherein the first and second main energy storing devices are further boosted to a third predetermined boost level by the fifth and sixth phase signals to allow the first and second main energy storing devices to output a desired level of a high-voltage signal through the first and second gating devices during the first and second phases.

23. (Currently Amended) A two-phase integrated circuit charge pump, comprising:

an oscillator, where the oscillator generates an oscillating signal during a phase cycle including [a] first and [a] second phases [phase];

a primary phase generator, coupled to the oscillator, wherein the primary phase generator generates [a] first [phase signal] and [a] second phase signals [signal] that are non-overlapping and crossing each other around high points of their signals during a phase cycle, further the primary phase generator generates [a] third [phase signal] and [a] fourth phase signals [signal] that are non-overlapping and crossing each other around low points of their signals during every phase cycle, and further the primary phase generator generates [a] seventh [phase signal] and [an] eighth phase signals [signal];

a secondary phase generator, coupled to the primary phase generator, wherein the secondary phase generator receives the first and second phase signals and generates [a] fifth [phase signal] and [a] sixth phase signals, respectively, [signal] that are non-overlapping and crossing each other around high points of their signals during a phase cycle and includes a predetermined delay from the first and second phase signals;

[a] first and second pre-boot precharge capacitors, coupled to the primary phase generator, wherein each of the first and second pre-boot precharge capacitors has an output, wherein the first and second pre-boot precharge capacitors receive the third and fourth phase signals from the primary phase generator during the first and second phases, respectively;

[a] first and second pre-boot capacitors, coupled to the primary phase generator [and the first and second pre-boot precharge capacitors respectively], wherein each of the first and second pre-boot capacitors has an output, wherein the output of each of the first and second pre-boot precharge capacitors is coupled to the output of the first and second preboot capacitors,

respectively, receives the first and second phase signals from the primary phase generator respectively, and wherein the first and second pre-boot precharge capacitors pre-charges the first and second pre-boot capacitors to a pre-determined level during the first and second phases respectively;

[a] first and second main pump precharge capacitors, coupled to the primary phase generator, wherein the first and second main pump precharge capacitors receive the seventh and eighth phase signals from the primary phase generator during the first and second phases respectively;

a first main pump capacitor, coupled to the first main pump precharge capacitor, the second pre-boot capacitor, and the secondary phase generator, wherein the first pre-boot capacitor pre-boots the first main pump to a predetermined booted level during the first phase, further the first main pump precharge capacitor precharges the first main pump capacitor to a second pre-determined level during the second phase and further the first main pump capacitor receives the fifth phase signal from the secondary phase generator during the first phase, and where the first main pump capacitor goes to a third predetermined level and outputs a charge through [to] a first p-channel gate during the first phase; and

a second main pump capacitor, coupled to the second main pump precharge capacitor, the first pre-boot capacitor, and the secondary phase generator, wherein the second pre-boot capacitor pre-boots the second main pump to a predetermined booted level during the second phase, further the second main pump precharge capacitor precharges the second main pump capacitor to a second pre-determined level during the first phase, and further the second main pump capacitor receives the sixth phase signal from the secondary phase generator during the second phase, and where the second main pump capacitor goes to the third predetermined level and outputs the charge through [to] a second p-channel gate during the second phase.

24. (Currently Amended) A two-phase charge pump for producing a pump voltage on an output line, comprising:

an oscillator, where the oscillator generates an oscillating signal;

a primary phase generator, coupled to the oscillator, generates [a] first [phase signal] and [a] second phase signals [signal] that are non-overlapping and crossing each other around high points of their signals during every phase cycle including first and second phases [(consisting of

a first phase and a second phase)], further the primary phase generator generates [a] third [phase signal] and [a] fourth phase signals [signal] that are non-overlapping and crossing each other around low points of their signals during every phase cycle, and further the primary phase generator generates [a] seventh [phase signal] and [a] eighth phase signals [signal];

a delay element, coupled to the primary phase generator, receives the first and second phase signals and generates [a] fifth [phase signal] and [a] sixth phase signals [signal] that are non-overlapping and crossing each other around high points of their signals during every phase cycle and includes a predetermined delay from the first and second phase signals;

a first and second pre-boot precharge circuitry, coupled to the primary phase generator, wherein the first and second pre-boot precharge circuitry has an output, receives the third and fourth signals from the primary phase generator during the [a] first and second phases respectively;

a first and second pre-boot circuitry, coupled to the primary phase generator and the first and second pre-boot precharge capacitors respectively, wherein the first and second pre-boot circuitry has an output, wherein the output of the first and second pre-boot precharge circuitry is coupled to the output of the first and second pre-boot circuitry, receives the first and second phase signals from the primary phase generator respectively, and wherein [where] the first and second pre-boot precharge circuitry pre-charges the first and second pre-boot capacitors to a pre-determined level during the first and second phases, respectively;

a first and second main pump precharge circuitry, coupled to the primary phase generator receives the seventh and eighth phase signals from the delay element during the first and second phases, respectively;

a first main pump circuitry, coupled to the first main pump precharge circuitry, the first pre-boot circuitry, and the delay element, where the first pre-boot circuitry pre-boots the first main pump circuitry to a predetermined booted level during the first phase, further the first main pump precharge circuitry precharges the first main pump circuitry to a second pre-determined level during the second phase and further the first main pump circuitry receives the fifth phase signal from the delay element during the first phase, and where the first main pump circuitry goes to a third predetermined level and outputs a charge through [to] a first p-channel gate during the first phase; and

a second main pump circuitry, coupled to the second main pump precharge circuitry, the second pre-boot circuitry, and the delay element, where the second pre-boot circuitry pre-boots the second main pump to a predetermined booted level during the second phase, further the second main pump precharge circuitry precharges the second main pump circuitry to a second pre-determined level during the first phase, and further the second main pump circuitry receives the sixth phase signal from the delay element during the second phase, and wherein [where] the second main pump circuitry goes to the third predetermined level and outputs the charge through [to] a second p-channel gate during the second phase.

25. (Currently Amended) A charge pump circuit, comprising:

a phase generator to generate [a] first [phase] and [a] second phases [phase], wherein the first phase is 180 degrees out of phase with respect to the second phase;

a primary phase generator, coupled to the oscillator, generates [a] first [phase signal] and [a] second phase signals [signal] that are non-overlapping and crossing each other around high points of their signals during every phase cycle including the first and second phases [(consisting of a first phase and a second phase)], further the primary phase generator generates [a] third [phase signal] and [a] fourth phase signals [signal] that are non-overlapping and crossing each other around low points of their signals during every phase cycle, and further the primary phase generator generates [a] seventh [phase signal] and [a] eighth phase signals [signal];

a secondary phase generator, coupled to the primary phase generator, receives the first and second phase signals and generates [a] fifth [phase signal] and [a] sixth phase signals, respectively, [signal] that are non-overlapping and crossing each other around high points of their signals during every phase cycle and includes a predetermined delay from the first and second phase signals;

[a] first and second pre-boot precharge capacitors, wherein each of the first and second pre-boot precharge capacitors has an output, coupled to the primary phase generator, receives the third and fourth signals from the primary phase generator during the [a] first and second phases respectively;

[a] first and second pre-boot capacitors, coupled to the primary phase generator [and the first and second pre-boot precharge capacitors, respectively], wherein each of the first and second pre-boot capacitors has an output, wherein the output of each of the first and second pre-

boot precharge capacitors is coupled to the output of the first and second pre-boot capacitors, respectively, receives the first and second phase signals from the primary phase generator respectively, and wherein [where] the first and second pre-boot precharge capacitors pre-charges the first and second pre-boot capacitors to a pre-determined level during the first and second phases, respectively;

[a] first and second main pump precharge capacitors, coupled to the primary phase generator receives the seventh and eighth phase signals from the primary phase generator during the first and second phases, respectively;

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a first main pump capacitor, coupled to the first main pump precharge capacitor, the first pre-boot capacitor, and the secondary phase generator, where the first pre-boot capacitor pre-boots the first main pump to a predetermined booted level during the first phase, further the first main pump precharge capacitor precharges the first main pump capacitor to a second pre-determined level during the second phase and further the first main pump capacitor receives the fifth phase signal from the secondary phase generator during the first phase, and where the first main pump capacitor goes to a third predetermined level and outputs a charge through [to] a first p-channel gate during the first phase; and

a second main pump capacitor, coupled to the second main pump precharge capacitor, the second pre-boot capacitor, and the secondary phase generator, where the second pre-boot capacitor pre-boots the second main pump to the [a] predetermined booted level during the second phase, further the second main pump precharge capacitor precharges the second main pump capacitor to the [a] second pre-determined level during the first phase, and further the second main pump capacitor receives the sixth phase signal from the secondary phase generator during the second phase, and where the second main pump capacitor goes to the third predetermined level and outputs the charge through [to] a second p-channel gate during the second phase.

26. (Currently Amended) A memory device, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

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27. (Currently Amended) A memory device, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, [; and]

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during [the] first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level [is] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

28. (Currently Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

29. (Currently Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

30. (Currently Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, [further] wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; [and]

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, [; and]

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during [the] first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level [is] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

31. (Currently Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

32. (Currently Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; [and]

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, [; and]

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during [the] first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level [is] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

33. (Currently Amended) An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

34. (Currently Amended) An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators, wherein each of the first and second preboot capacitors has an output;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; [and]

first and second pre-boot pre-charge capacitors, wherein each of the first and second pre-boot pre-charge capacitors has an output, and wherein the output of each of the first and second pre-boot pre-charge capacitors is coupled to the output of the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively, [; and]

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during [the] first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level [is] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively, wherein the first and second main pump capacitors output a pump voltage higher than a supply voltage through the first and second gating devices.

35. (Currently Amended) A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

recharging a pre-boot capacitor to a first pre-determined level during a first phase;

recharging a second pre-boot capacitor to the first pre-determined level during a second phase;

pre-charging a first main pump capacitor to a second pre-determined level during the second phase;

boosting the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a Vccp during the first phase through a first gating device;

pre-charging the second main pump capacitor to the second pre-determined level during the first phase;

boosting the second main pump to the third pre-determined level during the second phase; and

outputting the second main pump charge to the [a] Vccp during the second phase through a second gating device.

cont E1

36. (Currently Amended) A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

recharging a pre-boot capacitor to a first pre-determined level during a first phase;

recharging a second pre-boot capacitor to the first pre-determined level during a second phase;

pre-charging a first main pump capacitor to a second pre-determined level during the second phase;

boosting the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a Vccp through a first p-channel gate during the first phase;

pre-charging the second main pump capacitor to the second pre-determined level during the first phase;

boosting the second main pump to the third pre-determined level during the second phase; and

outputting the second main pump charge to the Vccp through a second p-channel gate during the second phase.

37. (Currently Amended) A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

recharging a pre-boot capacitor to a first pre-determined level during a first phase;

recharging a second pre-boot capacitor to the first pre-determined level during a second phase;

pre-charging a first main pump capacitor to a second pre-determined level during the second phase;

boosting the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a Vccp through a first p-channel gate during the first phase;

[outputting the charge from the first p-channel gate to a Vccp;]

pre-charging the second main pump capacitor to the second pre-determined level during the first phase;

boosting the second main pump to the third pre-determined level during the second phase; and

outputting the second main pump charge to the Vccp through a second p-channel gate during the second phase. [; and]

[outputting the charge from the second p-channel gate to a Vccp.]

38. (Currently Amended) A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

generating signals that are non-overlapping and crossing each other around high points of their signals;

generating signals that are non-overlapping and crossing each other around low points of their signals;

generating signals having a predetermined delay from the signals that are non-overlapping and crossing each other around high points;

recharging a first pre-boot capacitor to a first pre-determined level using the signals that are non-overlapping and crossing around the high points of their signals during a first phase;

recharging a second pre-boot capacitor to the first pre-determined level using the signals that are non-overlapping and crossing around the low points of their signals during a second phase;

pre-charging the first main pump capacitor to a second pre-determined level by the signals that are non-overlapping and crossing around the low points of their signals during the second phase;

inputting the signals having a predetermined delay to boost the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a first p-channel gate during the first phase;

outputting the charge from the first p-channel gate to a Vccp;

pre-charging the second main pump capacitor to the second pre-determined level by the signals that are non-overlapping and crossing around the low points of their signals during the first phase;

inputting the signals having a predetermined delay to boost the second main pump to the third pre-determined level during the second phase;

outputting the second main pump charge to a second p-channel gate during the second phase; and

outputting the charge from the second p-channel gate to the [a] Vccp.

39. (Currently Amended) A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

generating an oscillating signal;

generating a first and second phase signals that are non-overlapping and crossing each other around high points of their signals during every phase cycle from the oscillating signal by a primary phase generator;

generating a third and fourth phase signals that are non-overlapping and crossing each other around low points of their signals during every phase cycle from the oscillating signal by the primary phase generator;

generating a fifth and sixth phase signals having a predetermined delay from the first and second phase signals that are non-overlapping and crossing each other around high points from

the first and second phase signals received from the primary phase generator by a secondary phase generator;

generating a seventh and eighth phase signals by the primary phase generator;

recharging a first pre-boot capacitor to a first pre-determined level using the first and third phase signals during the first phase;

recharging a second pre-boot capacitor to the first pre-determined level using the second and fourth phase signals during the second phase;

pre-booting a first main pump capacitor to the pre-determined boot level by the first pre-boot capacitor during the first phase;

pre-booting a second main pump capacitor to a pre-determined boot level by the second pre-boot capacitor during the second phase;

pre-charging the first main pump capacitor to a second pre-determined level by the seventh phase signal during the second phase;

inputting the fifth phase signal to boost the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a first p-channel gate during the first phase;

outputting the charge from the first p-channel gate to a Vccp;

pre-charging the second main pump capacitor to the second pre-determined level by the eight phase signal during the first phase;

inputting the sixth phase signal to boost the second main pump to the third pre-determined level during the second phase;

outputting the second main pump charge to a second p-channel gate during the second phase; and

outputting the charge from the second p-channel gate to the [a] Vccp.

40. (Currently Amended) A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

generating an oscillating signal;

generating a first and second phase signals that are non-overlapping and crossing each other around high points of their signals during every phase cycle from the oscillating signal by a primary phase generator;

generating a third and fourth phase signals that are non-overlapping and crossing each other around low points of their signals during every phase cycle from the oscillating signal by the primary phase generator;

generating a fifth and sixth phase signals having a predetermined delay of approximately in the range of about 10 to 30 nanoseconds from the first and second phase signals that are non-overlapping and crossing each other around high points from the first and second phase signals received from the primary phase generator by a secondary phase generator;

generating a seventh and eighth phase signals by the primary phase generator;

recharging a first pre-boot capacitor to a first pre-determined level of approximately in the range of about 1 to 5 volts using the first and third phase signals during the first phase;

recharging a second pre-boot capacitor to the first pre-determined level of approximately in the range of about 1 to 5 volts using the second and fourth phase signals during the second phase;

pre-booting a first main pump capacitor to the pre-determined boot level of approximately in the range of about 1 to 5 volts by the first pre-boot capacitor during the first phase;

pre-booting a second main pump capacitor to a pre-determined boot level of approximately in the range of about 1 to 5 volts by the second pre-boot capacitor during the second phase;

pre-charging the first main pump capacitor to a second pre-determined level of approximately in the range of about 1 to 5 volts by the seventh phase signal during the second phase;

inputting the fifth phase signal to boost the first main pump to a third pre-determined level of approximately in the range of about 1 to 5 volts during the first phase;

outputting the first main pump charge to a first p-channel gate during the first phase;

outputting the charge from the first p-channel gate to a Vccp;

pre-charging the second main pump capacitor to the second pre-determined level approximately in the range of about 1 to 5 volts by the eight phase signal during the first phase;

inputting the sixth phase signal to boost the second main pump to the third pre-determined level of approximately in the range of about 1 to 5 volts during the second phase;

outputting the second main pump charge to a second p-channel gate during the second phase; and

outputting the charge from the second p-channel gate to the [a] Vccp.

41. (Currently Amended) A method of producing a pump supply voltage in an integrated circuit, the method, comprising:

generating an oscillating signal;

generating a first and second phase signals that are non-overlapping and crossing each other around high points of their signals during every phase cycle from the oscillating signal by a primary phase generator;

generating a third and fourth phase signals that are non-overlapping and crossing each other around low points of their signals during every phase cycle from the oscillating signal by the primary phase generator;

generating a fifth and sixth phase signals from the first and second phase signals, where the fifth and sixth phase signals are similar to the first and second phase signals, and having a predetermined delay from the first and second phase signals by a secondary phase generator;

generating a seventh and eighth phase signals by the primary phase generator;

recharging a first pre-boot capacitor to a first pre-determined level using the first and third phase signals during the first phase;

recharging a second pre-boot capacitor to the first pre-determined level using the second and fourth phase signals during the second phase;

pre-booting a first main pump capacitor to the pre-determined boot level by the first pre-boot capacitor during the first phase;

pre-booting a second main pump capacitor to a pre-determined boot level by the second pre-boot capacitor during the second phase;

recharging the first main pump capacitor to a second pre-determined level by the seventh phase signal during the second phase;

inputting the fifth phase signal to raise the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a Vccp through a first gating device during the first phase;

pre-charging the second main pump capacitor to the second pre-determined level by the eight phase signal during the first phase;

inputting the sixth phase signal to raise the second main pump to the third pre-determined level during the second phase; and

outputting the second main pump charge to the Vccp through a second gating device during the second phase.

42. (Previously Added) The charge pump of claim1, further comprising:

first and second sharing transistors coupled to the first and second pre-boot pre-charge capacitors and the first and second pre-boot capacitors to provide a path that charge shares the first and second pre-boot capacitors to the first and second main pump capacitors.